Amendments to the CLAIMS:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

LISTING OF CLAIMS:

1. (Currently Amended) An ATM switch comprising:

at least one basic switch, said basic switch including means for referring to time information written in a header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including:

plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including:

an address filter for extracting a cell arriving from the input line;

a first buffer which stores the extracted cell;

a second buffer which stores a cell arriving from another cross-point; and

means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port;

wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer.

2. (Currently Amended) An ATM switch comprising:

a first stage;

a second stage; and

a third stage, wherein each of the stages includes at least one basic switch, wherein said first stage, said second stage and said third stage are connected, said basic switch including means for referring to time information written in a header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including:

plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including:

an address filter for extracting a cell arriving from the input line;

a first buffer which stores the extracted cell;

a second buffer which stores a cell arriving from another cross-point; and

means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port;

wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer.

3. (Canceled).

4. (Previously Presented) The ATM switch as claimed in claim 1,

wherein input lines connected to the cross-points are classified into a plurality of groups,

said first buffer storing cells arriving from said input lines of one of said groups;

time information of a cell with the earliest time information among cells in said first buffer being compared with time information of said head cell in said second buffer, and

a cell with earlier time information being sent to a cross-point or said output port.

5. (Original) The ATM switch as claimed in claim 1, further comprising adding means which adds arriving time information to an arriving cell as said time information.

6. (Original) The ATM switch as claimed in claim 5, wherein said adding means generates a dummy cell and adds time information to said dummy cell if there is no input cell.

7. (Original) The ATM switch as claimed in claim 6, wherein said basic switch transfers said dummy cells or said arriving cells with said time information to output ports other than the destination of said arriving cell.

8. (Original) The ATM switch as claimed in claim 7, wherein said basic switch allows said dummy cell to be overwritten by an arriving cell.

9. (Original) The ATM switch as claimed in claim 5,

wherein said time information is a value repeating periodically;

said adding means adding a flag for identifying said period to said cell, and

said basic switch identifying said period by referring to said flag.

10. (Original) The ATM switch as claimed in claim 1, wherein said basic switch includes a delay time counter, adds said delay time, and uses said added delay time as said time information.

11. (Currently Amended) A large-sized ATM switch comprising:

interconnected ATM switches each of which ATM switches includes at least one basic switch, said basic switch including means for referring to time information written in a header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including:

plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including:

an address filter for extracting a cell arriving from the input line;

a first buffer which stores the extracted cell;

a second buffer which stores a cell arriving from another cross-point; and

means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port;

wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer.

12-26. (Canceled).

27. (Currently Amended) A cell switch comprising:

at least one basic switch, said basic switch including means for referring to time information written in a header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including:

plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including:

an address filter for extracting a cell arriving from the input line;

a first buffer which stores the extracted cell;

a second buffer which stores a cell arriving from another cross-point; and

means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port;

wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer.

28. (Canceled).

29. (Currently Amended) A large-sized cell switch comprising:

interconnected cell switches, wherein each of the cell switches includes at least one basic switch, said basic switch including means for referring to time information written in a

header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including:

plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including:

an address filter for extracting a cell arriving from the input line;

a first buffer which stores the extracted cell;

a second buffer which stores a cell arriving from another cross-point; and

means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port;

wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell, or said dummy cell in said first buffer.

30-34. (Canceled).

35. (Currently Amended) A basic switch which inputs a cell and outputs said cell to an output port on the basis of header information of said cell, said basic switch comprising:

means for referring to time information written in a header of an input cell and for switching cells to an output port in an ascending order of said time information, said means including:

plural cross-points, wherein at each of the cross-points an input line and an output line are crossed, and wherein the plural cross-points are layered, each cross-point including:

an address filter for extracting a cell arriving from the input line;

a first buffer which stores the extracted cell;

a second buffer which stores a cell arriving from another cross-point; and

means for comparing time information of a head cell in said first buffer with time information of a head cell in said second buffer and for sending a head cell with earlier time information to the another cross-point or said output port;

wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer.

36. (Canceled).

37-40. (Canceled).

41. (Previously Presented) The ATM switch as claimed in claim 1, wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer,

if types of head cells in said first buffer and said second buffer are the same and also time information of said head cells are the same, a k-th cross point selects a head cell from said first buffer and said second buffer with a probability of a ratio of 1 to k-1 so as to send a selected head cell to the another cross-point or said output port, wherein k is a natural number, and

if said types of head cells are different but time information are the same, said address filter selects said actual cell so as to send said actual cell to other cross-point or said output port.

42. (Previously Presented) The ATM switch as claimed in claim 2, wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer,

if types of head cells in said first buffer and said second buffer are the same and also time information of said head cells are the same, a k-th cross point selects a head cell from said first buffer and said second buffer with a probability of a ratio of 1 to k-1 so as to send a

selected head cell to the another cross-point or said output port, wherein k is a natural number, and

if said types of head cells are different but time information are the same, said address filter selects said actual cell so as to send said actual cell to other cross-point or said output port.

43. (Previously Presented) The large-sized ATM switch as claimed in claim 11, wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer,

if types of head cells in said first buffer and said second buffer are the same and also time information of said head cells are the same, a k-th cross point selects a head cell from said first buffer and said second buffer with a probability of a ratio of 1 to k-1 so as to send a selected head cell to the another cross-point or said output port, wherein k is a natural number, and

if said types of head cells are different but time information are the same, said address filter selects said actual cell so as to send said actual cell to other cross-point or said output port.

44. (Previously Presented) The cell switch as claimed in claim 27, wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer,

if types of head cells in said first buffer and said second buffer are the same and also time information of said head cells are the same, a k-th cross point selects a head cell from said first buffer and said second buffer with a probability of a ratio of 1 to k-1 so as to send a selected head cell to the another cross-point or said output port, wherein k is a natural number, and

if said types of head cells are different but time information are the same, said address filter selects said actual cell so as to send said actual cell to other cross-point or said output port.

45. (Previously Presented) The large-sized cell switch as claimed in claim 29, wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell, or said dummy cell in said first buffer,

if types of head cells in said first buffer and said second buffer are the same and also time information of said head cells are the same, a k-th cross point selects a head cell from said first buffer and said second buffer with a probability of a ratio of 1 to k-1 so as to send a selected head cell to the another cross-point or said output port, wherein k is a natural number, and

if said types of head cells are different but time information are the same, said address filter selects said actual cell so as to send said actual cell to other cross-point or said output port.

46. (Previously Presented) The basic switch as claimed in claim 35, wherein said address filter captures a cell having an address of said address filter as an actual cell, and generates, for a cell that does not have said address of said address filter, a dummy cell with time information of the cell, and stores said actual cell or said dummy cell in said first buffer,

if types of head cells in said first buffer and said second buffer are the same and also time information of said head cells are the same, a k-th cross point selects a head cell from said first buffer and said second buffer with a probability of a ratio of 1 to k-1 so as to send a selected head cell to the another cross-point or said output port, wherein k is a natural number, and

if said types of head cells are different but time information are the same, said address filter selects said actual cell so as to send said actual cell to other cross-point or said output port.